Interfacing the 3-volt DataFlash® with a 5-volt System

DataFlash®

Application Note

Overview

As semiconductor processes transition to deep sub-micron lithography, supply voltages need to be reduced accordingly. The transition from 5-volt supply systems to 3-volt systems is accelerating in the current market place. However, not all components have migrated to the lower voltage and system designers are encountering difficulty specifying the entire bill of materials in a single-power supply range. This is an even greater problem for companies facing maintenance of legacy systems and spares sourcing where complete redesigns are not practical or due to obsolescence of the original 5-volt parts.

Atmel has kept this in mind when designing the AT45DBxxxx Series, 3-volt only DataFlash family. The 3-volt DataFlash family can be used in 5-volt systems. This application note discusses the conditions for using a 3-volt DataFlash device in a 5-volt system or in systems with mixed voltage environment.

AC Characteristics and Operational Conditions

Supply Voltage Requirements

The power supply to the DataFlash device must be between 2.7V and 3.6V for correct operation. Exceeding these levels may result in incorrect operation or cause damage to the device. Max ratings are shown in the DC/AC Operating Range and Absolute Maximum ratings tables in the datasheets.

Logic Level Definitions

Currently, the majority of systems conform to one or two logic interfacing standards, these being TTL or CMOS. Therefore, it is necessary to consider the effects of interfacing a 3-volt DataFlash to a 5-volt system that is either CMOS or TTL compatible.

TTL Logic Levels

The minimum V_{IH} requirement of a TTL-compatible input is 2.0V to register a logic 1, and the V_{IL} requirement of a TTL-compatible input is 0.8V to register a logic 0. Refer to the manufacturers datasheet to ensure full compliance with the input and output logic level requirements.

CMOS Logic Levels

The minimum V_{IH} requirement for a CMOS-compatible input is 0.7 x V_{CC} to register a logic 1, where V_{CC} is the supply voltage of the input device. For a CMOS device operating with a V_{CC} of 4.5V to 5.5V, this gives a V_{IH} requirement of 3.15V to 3.85V. The V_{IL} requirement of a CMOS-compatible input is 0.2 x V_{CC} to register a logic 0. This gives a V_{IL} requirement of 0.9V to 1.1V.

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System Considerations and Problem Definition

To fully review the implications of operating a 3-volt DataFlash device in a 5-volt system, the following two aspects need to be considered.

1. Device Input and Output Level Requirements
2. Voltage Regulation to the DataFlash

Device Input and Output Level Requirements

The DataFlash input pins are tolerant to 5-volt input levels and will not present a problem in either CMOS or TTL-compatible systems. The input and output pins for the DataFlash are shown below.

DataFlash Input Pins

SI	Serial Data In
SCK	Serial Clock
$\overline{CS}$	Chip Select
Reset	Reset Input
$\overline{WP}$	Write Protect

DataFlash Output Pins

SO	Serial Data Out(1)
I/O7 - I/O0(1)	Parallel Data Out (Bit 7 through Bit 0)
RDY/$\overline{BUSY}$	Ready Busy Signal

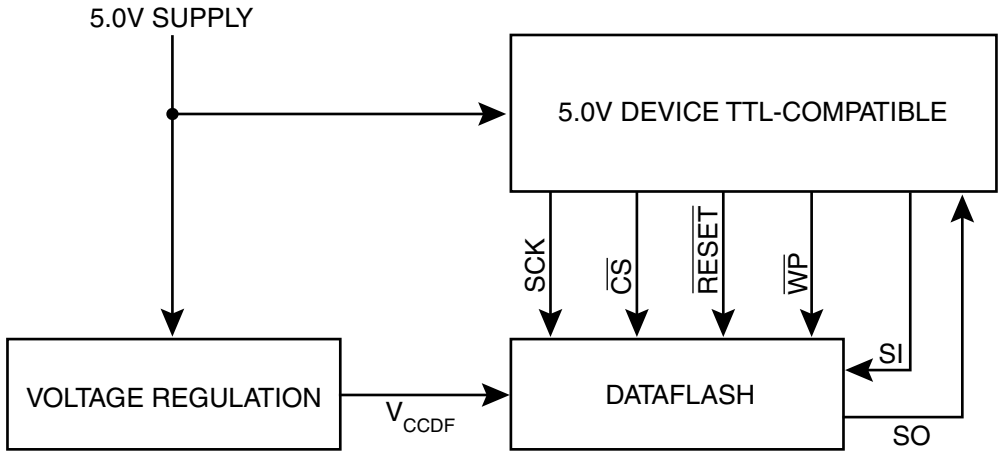
Note: 1. This application note will only consider Serial data mode. The Parallel data mode option is not available on all devices.

The output pins, however, will only operate within the specification of the DataFlash and the limits of the V_{CCDF} power supply. The DataFlash has one output pin in Serial data mode and 8 output pins in Parallel data mode. The RDY/$\overline{BUSY}$ signal is an open collector output indicating the current status of the device. The RDY/$\overline{BUSY}$ pin can be connected to 5-volt supply via a 1 kΩ external pull-up resistor.

Driving a TTL-compatible Load

A DataFlash driving into a TTL-compatible input will meet minimum TTL input logic level requirements. The DataFlash output will drive to V_{CCDF} – 0.2V. Therefore, under worst case or lowest V_{CCDF} conditions, the minimum output level achievable by the DataFlash will be V_{OH} = 2.7V - 0.2V = 2.5V. Figure 1 illustrates a typical system where the DataFlash is driving a TTL-compatible load.

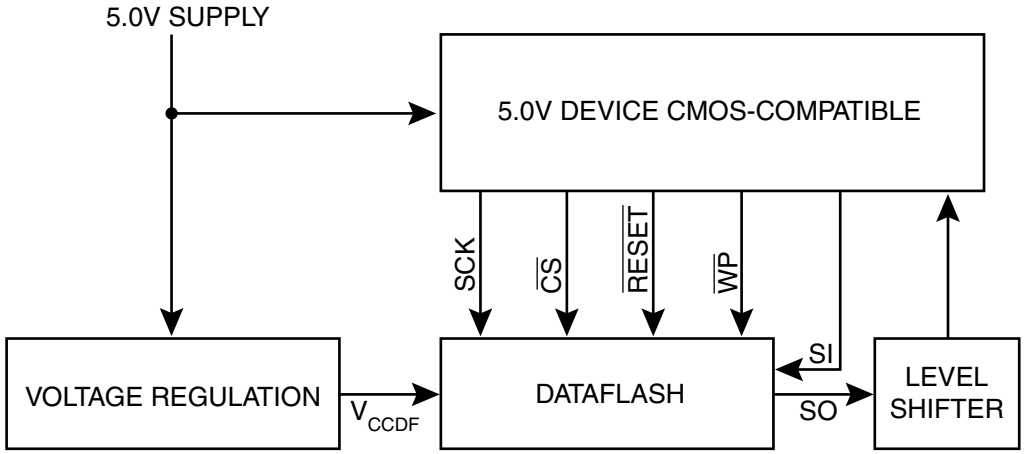
Figure 1. TTL-compatible Device Interface Diagram



Driving a CMOS-compatible Load

A problem arises when considering the output drive levels provided by the Serial output pin (SO) of a DataFlash when driving into a CMOS-compatible interface. A standard 5V compatible CMOS input requires a V_{IH} input of 3.15V minimum, greater than the output drive level that DataFlash can provide under worst-case conditions. Since the output of the DataFlash is not capable of driving a 5V CMOS load directly, a Level Shifter or alternative method of translating the DataFlash output logic levels to those compatible with the input device is required. Figure 2 illustrates the requirement for a Level Shifter in the Serial data output signal path of the DataFlash when driving a 5V compatible CMOS input.

Figure 2. CMOS-compatible Interface Diagram



Voltage Regulation

Few systems will provide both 5V and 3V regulated V_{CC} rails in the same circuit; therefore, a system or method to step down and regulate the voltage to the DataFlash is required. The choice of voltage regulator depends on the host system power supply characteristics, the maximum current drawn by the DataFlash device, and the costs associated with adding a voltage regulator. In legacy systems this may also require additional thought towards the practical implementation of the chosen solution.

Programming Current

It is essential to consider the maximum current requirements of the DataFlash when selecting an appropriate method of voltage regulation. Maximum load or peak current draw occurs when the DataFlash is in programming or erase mode and can range from 70 mA to 80 mA. It is also important to consider RMS current requirements of the DataFlash during these operations. Current starvation will increase noise in the whole system and also lead to the incorrect operation and possible data corruption in the DataFlash device during programming or erase operations.

System Solutions

By ensuring that the input signals to the 3V only DataFlash devices remain 5-volt tolerant, Atmel has minimized the overall impact on the end applications and customers. However, two issues have been identified in the discussion above when attempting to use a DataFlash device in a 5-volt system as follows:

- A secondary Voltage Regulator will be required.
- A Level Shifter will be required to translate the output logic level of the DataFlash output when used in a 5-volt CMOS-compatible system.

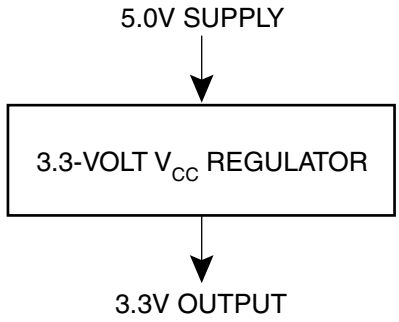
Practical and workable solutions for these two issues will be wide ranging and many innovative solutions will be found. The following section will look at some of the more conventional possibilities.

Voltage Regulation Solutions

A Simple Voltage Regulator Option

Many off-shelf-voltage regulators or DC-to-DC converters exist today that would provide the DataFlash with a 2.7V to 3.6V regulated V_{CC} supply from an input supply range of 4.5V to 5.5V. Figures 3 and 4 illustrate a typical voltage regulator solution utilizing a Linear Technology LT1761 Series Low Drop Out, Low Noise regulator.

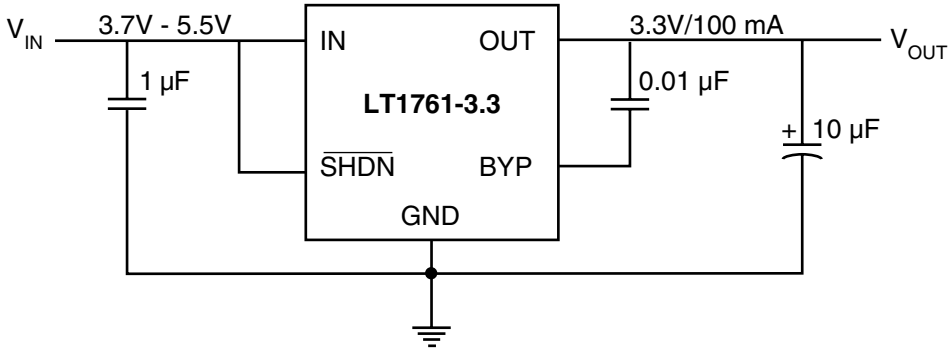
Figure 3. Voltage Regulator Diagram



Linear Technologies LT1761 Series Regulator

Other solutions could be implemented using a wide range of single-chip voltage regulators or converters available from different manufacturers. Table 1, on page 7, provides a short list of semiconductor manufacturers offering voltage regulators or DC-to-DC converters suitable for this application. Any voltage regulator-based design would need to consider current delivery requirements and may require additional external components such as capacitors, resistors or inductors to ensure correct operation, regulation and current delivery. Please consult appropriate vendors datasheets and applications notes on the individual components.

Figure 4. Example Voltage Regulator Solution



A Simple Diode Voltage Converter

Figures 5 and 6 illustrate a simple three-diode regulator scheme. The threshold voltage (V_t = 0.7V approx.) for each diode would contribute to a total series voltage drop across the circuit of 2.1 volts. The advantage to this kind of regulation scheme is cost and space. One limitation of this circuit is the input voltage range, which must remain at or above 4.8V to ensure a minimum supply at the DataFlash remains above 2.7V. Selecting diodes with higher or lower V_t thresholds would allow for finer tuning of the circuit operation.

Figure 5. Example of a Simple Diode Voltage Regulator

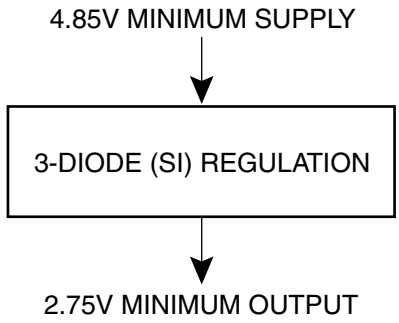
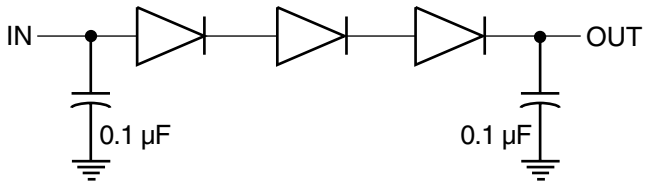


Figure 6. Simple Diode Regulator Circuit Diagram

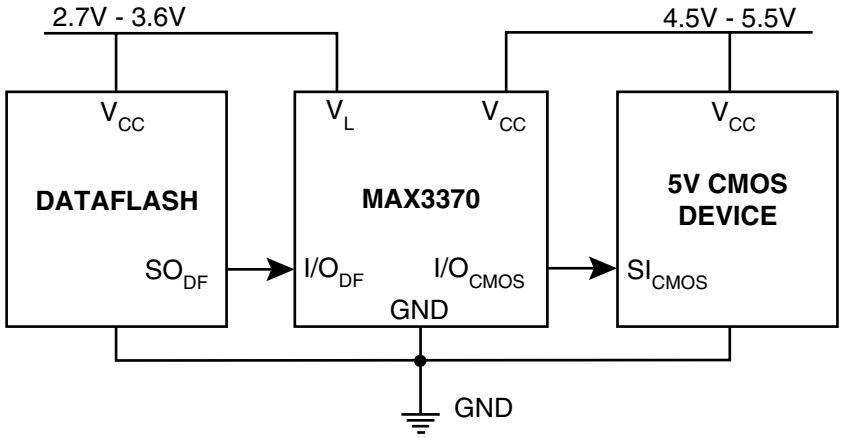


Output Voltage Level Translation Solutions

The Maxim MAX3370 Logic Level Translator

The circuit illustrated in Figure 7, utilizes a Maxim MAX3370 Level translator circuit to level shift the low voltage output of the DataFlash device to a high voltage output (V_{IH}) compatible with the 5V CMOS circuit. It should be noted that the MAX3370 does not allow the I/O to float and this will cause difficulties in systems where multiple bus masters drive the SPI bus. To allow multiple bus masters to operate correctly on any given SPI bus, each controller or slave device will need to allow the bus signals to float. In a normal situation where the DataFlash is directly connected to any number of bus masters, the DataFlash output will float when the device chip select pin is high. With the MAX3370 in circuit, and although the DataFlash output is floating, the MAX3370 continues to drive the level shifted I/O either high or low causing a potential bus conflict. In the event that the system will require multiple master devices on the same SPI bus as the DataFlash then the circuit shown in Figure 8 will be more effective.

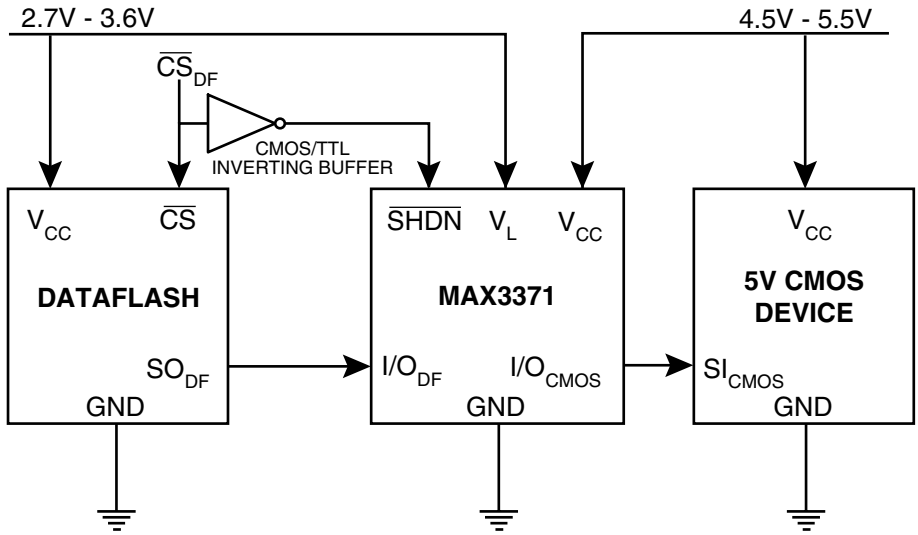
Figure 7. Maxim MAX3370 Voltage Level Translator



The Maxim MAX3371 Logic Level Translator

The circuit illustrated in Figure 8, uses the MAX3371 Level Translator. This device includes an active low output control pin $\overline{SHDN}$ to allow the bi-directional I/O pins of the chip to float when not in use by disconnecting the internal pull-up resistor. To disable or float the DataFlash I/O, the chip select pin on the DataFlash must be taken high. Therefore, it will be necessary to add an additional inverter to the circuit between the DataFlash chip select and $\overline{SHDN}$ to facilitate full multi-master bus capability. The MAX3370 and MAX3371 circuits are capable of 2 Mbps data transfer rates, which should be suitable for the majority of applications.

Figure 8. A Maxim MAX3371 Level Translator with Floating IO



The ON Semiconductor MC74VHC1GT Non-Inverting Buffer

An alternative to the level translation solutions shown in Figures 7 and 8 above is the ON semiconductor MC74VHC1GT non-inverting buffer. This device provides full logic level translation, maintaining full CMOS and TTL compatibility. The device also incorporates an output enable function allowing the output to float supporting multiple bus master operation. As the $\overline{OE}$ pin must be driven high to disable the outputs, it is compatible with the DataFlash chip select logic level negating the need for an additional inverter as required in the MAX3371 circuit.

Figure 9. ON Semiconductor MC74VHC1GT Buffer

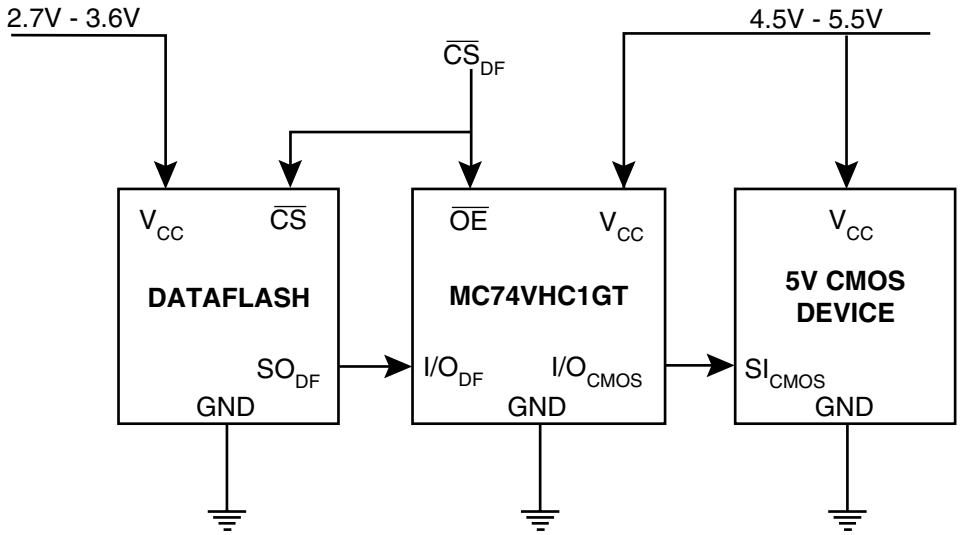


Table 1 provides a short list of semiconductor manufacturers offering Level translators suitable for this application.

Table 1. A Short List of Potential Voltage Regulator and Level Translator Manufacturers

Function	Manufacturer	Web Site
Voltage Regulation	Linear Technology	www.linear-tech.com
Voltage Regulation	Texas Instrument	www.ti.com
Voltage Regulation	Analog Devices	www.analog.com
Level Translators	Maxim	www.maxim-ic.com
Level Translators	Dallas Semiconductor	www.dalsemi.com
Level Translators	ON Semiconductor	www.onsemi.com

Conclusion

As this application note detailed, Atmel's AT45DBxxxx 3-volt DataFlash family can be easily interfaced to 5-volt devices in new systems or where legacy designs need to be supported. The system designer needs only to account for the proper I/O levels on the output side of the DataFlash device, peak current requirements during erase/programming cycles and V_{CC} supply voltage demands. The solution to over come the differences in interface voltages will be determined ultimately by several factors, cost, space, practicality, system specification and performance. The scope of these changes has been minimized by Atmel's advance consideration of the impact of essential technology migration and evolution by ensuring that the DataFlash inputs remain 5-volt tolerant irrespective of supply voltage.

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