INTRODUCTION

Ceramic chips consist of formulated ceramic dielectric materials which have been fabricated into thin layers, interspersed with metal electrodes alternately exposed on opposite edges of the laminated structure. The entire structure is then fired at high temperature to produce a monolithic block which provides high capacitance values in a small physical volume. After firing, conductive terminations are applied to opposite ends of the chip to make contact with the exposed electrodes. Standard end terminations use a nickel barrier layer and a tin overplate to provide excellent solderability for the customer.

KEMET multilayer ceramic chip capacitors are produced in plants designed specifically for chip capacitor manufacture. The process features a high degree of mechanization as well as precise controls over raw materials and process conditions. Manufacturing is supplemented by extensive Technology, Engineering and Quality Assurance programs.

KEMET ceramic chip capacitors are offered in the five most popular temperature characteristics. These are designated by the Electronics Industries Association (EIA) as the ultra-stable C0G (also known as NP0, military version BP), the stable X7R (military BX or BR), the stable X5R, and the general purpose Z5U and Y5V. A wide range of sizes are available. KEMET multilayer ceramic chip capacitors are available in KEMET's tape and reel packaging, compatible with automatic placement equipment. Bulk cassette packaging is also available (0805,0603 and 0402 only) for those pick and place machines requiring its use.

ELECTRICAL CHARACTERISTICS

1. Working Voltage:

Refers to the maximum continuous DC working voltage permissible across the entire operating temperature range. The reliability of multilayer ceramic capacitors is not extremely sensitive to voltage, and brief applications of voltage above rated will not result in immediate failure. However, reliability will be degraded by sustained exposure to voltages above rated.

2. Temperature Characteristics:

Within the EIA classifications, various temperature characteristics are identified by a three-symbol code; for example: C0G, X7R, X5R, Z5U and Y5V.

For Class I temperature compensating dielectrics (includes C0G), the first symbol designates the significant figures of the temperature coefficient in PPM per degree Celsius, the second designates the multiplier to be applied, and the third designates the tolerance in PPM per degrees Celsius. EIA temperature characteristic codes for Class I dielectrics are shown in Table 1.

Table 1 – EIA Temperature Characteristic Codes for Class I Dielectrics

Significant Figure of Temperature Coefficient		Multiplier Applied to Temperature Coefficient		Tolerance of Temperature Coefficient	
PPM per Degree C	Letter Symbol	Multiplier	Number Symbol	PPM per Degree C	Letter Symbol
0.0	C	-1	0	± 30	G
0.3	B	-10	1	± 60	H
0.9	A	-100	2	± 120	J
1.0	M	-1000	3	± 250	K
1.5	P	-10000	4	± 500	L

KEMET supplies the C0G characteristic.

For Class II and III dielectrics (including X7R, X5R, Z5U & Y5V), the first symbol indicates the lower limit of the operating temperature range, the second indicates the upper limit of the operating temperature range, and the third indicates the maximum capacitance change allowed over the operating temperature range. EIA type designation codes for Class II and III dielectrics are shown in Table 2.

Table 2 – EIA Temperature Characteristic Codes for Class II & III Dielectrics

Low Temperature Rating		High Temperature Rating		Maximum Capacitance Shift		
Degree Celsius	Letter Symbol	Degree Celsius	Number Symbol	Percent	Letter Symbol	EIA Class
+10C	Z	+45C	2	± 1.0%	A	II
-30C	Y	+65C	4	± 1.5%	B	II
-55C	X	+85C	5	± 2.2%	C	II
		+105C	6	± 3.3%	D	II
		+125C	7	± 4.7%	E	II
		+150C	8	± 7.5%	F	II
		+200C	9	± 10.0%	P	II
				± 15.0%	R	II
				± 22.0%	S	III
				+ 22/-33%	T	III
				+22/-56%	U	III
				+22/-82%	V	III

KEMET supplies the X7R, X5R, Z5U and Y5V characteristics.

3. Capacitance Tolerance:

See tables on pages 73-76.

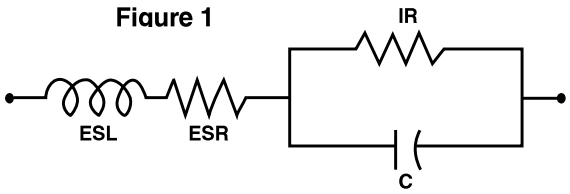
4. Capacitance:

Within specified tolerance when measured per Table 3.

The standard unit of capacitance is the farad. For practical capacitors, capacitance is usually expressed in microfarads (10^{-6} farad), nanofarads (10^{-9} farad), or picofarads (10^{-12} farad). Standard measurement conditions are listed in Table 3 - Specified Electrical Limits.

Like all other practical capacitors, multilayer ceramic capacitors also have resistance and inductance. A simplified schematic for the single frequency equivalent circuit is shown in Figure 1. At high frequency more complex models apply - see KEMET SPICE models at www.kemet.com for details.

Figure 1



C = Capacitance
ESR = Equivalent Series Resistance
ESL = Equivalent Series Inductance
IR = Insulation Resistance

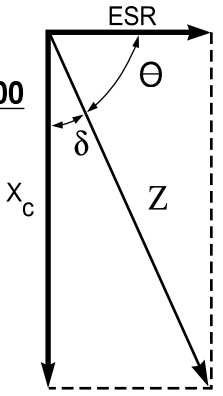
5. Dissipation Factor:
Measured under same conditions as capacitance. (See Table 3)

Dissipation factor (DF) is a measure of the losses in a capacitor under AC application. It is the ratio of the equivalent series resistance to the capacitive reactance, and is usually expressed in percent. It is normally measured simultaneously with capacitance, and under the same conditions. The vector diagram below illustrates the relationship between DF, ESR and impedance. The reciprocal of the dissipation factor is called the "Q" or quality factor. For convenience, the "Q" factor is often used for very low values of dissipation factor especially when measured at high frequencies. DF is sometimes called the "loss tangent" or "tangent δ", as shown in Figure 2.

Figure 2

$$DF(\%) = \frac{ESR \times 100}{X_C}$$

$$X_C = \frac{1}{2\pi fC}$$



6. Impedance:

Since the parallel resistance (IR) is normally very high, the total impedance of the capacitor can be approximated by:

Figure 3

$$Z = \sqrt{ESR^2 + (X_L - X_C)^2}$$

Where: Z = Total Impedance

ESR = Equivalent Series Resistance

X_C = Capacitive Reactance = $1/(2\pi fC)$

X_L = Inductive Reactance = $(2\pi f)(ESL)$

The variation of a capacitor's impedance with frequency determines its effectiveness in many applications. At high frequency more detailed models apply - see KEMET SPICE models for such instances.

7. Insulation Resistance:
Measured after 2 minutes electrification at 25°C and rated voltage: Limits per Table 3.

Insulation Resistance is the measure of a capacitor to resist the flow of DC leakage current. It is sometimes referred to as "leakage resistance". Insulation resistance (IR) is the DC resistance measured across the terminals of a capacitor, represented by the parallel resistance (IR) shown in Figure 1. For a given dielectric type, electrode area increases with capacitance, resulting in a decrease in the insulation resistance. Consequently, insulation resistance limits are usually specified as the "RC" (IR x C) product, in terms of ohm-farads or megohm-micro-farads. The insulation resistance for a specific capacitance value is determined by dividing this product by the capacitance. However, as the nominal capacitance values become small, the insulation resistance calculated from the RC product reaches values which are impractical. Consequently, IR specifications usually include both a minimum RC product and a maximum limit based on the IR calculated

Table 3 – Specified Electrical Limits

Parameter	Temperature Characteristics			
	C0G	X7R/X5R	Z5U	Y5V
Capacitance & Dissipation Factor: Measured at following conditions: C0G – 1kHz and 1 vrms if capacitance >1000 pF 1MHz and 1 vrms if capacitance ≤1000 pF X7R/X5R/Y5V – 1kHz and 1 vrms* if capacitance ≤ 10 µF X7R/X5R/Y5V – 120Hz and 0.5 vrms if capacitance > 10 µF Z5U – 1kHz and 0.5 vrms				
DF Limits: **X5R / Cap / DF: <25V / <564 / 5.0%; <25V / ≥564 / 10.0%; 50 - 200 volts; 25 volts; 16 volts; 6.3/10 volts	0.10% 0.10% -------- --------	2.5% 2.5% 3.5% 5.0% 3.5% ** 5.0% **	4.0% 4.0% -------	5.0% 7.0% 7.0% 10.0%
Dielectric Strength: At 2.5 times rated DC voltage	Pass Subsequent IR Test			
Insulation Resistance (IR): At rated DC voltage, whichever of the two is smaller. To get IR limit, divide MΩ–µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.	1,000 MΩ – µF or 100 GΩ (100,000 MΩ)	1,000 MΩ – µF or 100 GΩ (100,000 MΩ)	100 MΩ – µF or 10 GΩ (10,000 MΩ)	100 MΩ – µF or 10 G (≥16 volt) 50 MΩ – µF or 10G (≤10v) (10,000 MΩ)
Temperature: Range, °C Capacitance Change (without DC voltage)	-55 to +125 0 ± 30 ppm/°C	X7R: -55 to +125 ±15% X5R: -55 to +85 ±15%	+10 to +85 +22% -56%	-30 to +85 +22% -82%

***Note: Some values measured at ½ volt, see X7R Table for specific details on pages 74 and 75.**

from that value. For example, a typical IR specification might read "1,000 megohm-microfarads or 100 gigohms, whichever is less". The DC leakage current may be calculated by dividing the applied voltage by the insulation resistance (Ohm's Law).

8. Dielectric Withstanding Voltage:
250% of rated voltage for 5 seconds with current limited to 50mA at 25°C. Limits per Table 3.

Dielectric withstanding voltage (DWV) is the peak DC voltage which a capacitor is designed to withstand without damage for short periods of time. All KEMET multilayer ceramic surface mount capacitors will withstand a DC test voltage of 2.5 x the rated voltage for 60 seconds.

KEMET specification limits for all electrical characteristics at standard measurement conditions are shown in Table 3. Variations in these properties caused by changing conditions (temperature, voltage, frequency, and time) are covered in the following sections.

9. Aging Rate:
Maximum % Capacitance Loss/Decade Hour
C0G - 0%
X7R - 2.0%
X5R - 5.0%
Z5U - 7.0%
Y5V - 7.0%
Actual rates may be lower. Consult factory for details.

The capacitance of Class II and III dielectric changes with time as well as with temperature, voltage and frequency. The change with time is known as "aging". It is caused by gradual realignment of the crystalline structure of the ceramic dielectric material as it is cooled below its Curie temperature, which produces a loss of capacitance with time. The aging process is predictable and follows a logarithmic decay.

The aging process is reversible. If the capacitor is heated to a temperature above its Curie point for some period of time, de-aging will occur and the capacitor will regain the capacitance lost during the aging process. The amount of de-aging depends on both the elevated temperature and the length of time at that temperature. Exposure to 150°C for one-half hour is sufficient to return the capacitor to its initial value.

Because the capacitance changes rapidly immediately after de-aging, capacitance measurements are indexed to a referee time of 1,000 hours. All Kemet capacitors are shipped to be within tolerance at the referee time of 1,000 hours after the deaging process (this time is often referred to as "last heat"). The selection of this referee time has proven practical, as the actual decline of capacitance after 1,000 hours is very low.

10. Effect of Temperature:

Both capacitance and dissipation factor are affected by variations in temperature. The maximum capacitance change with temperature is defined by the temperature characteristic.

However, this only defines an "envelope" bounded by the upper and lower operating temperatures and the minimum and maximum capacitance values. Within this "envelope", the variation with temperature depends upon the specific dielectric formulation.

Insulation resistance decreases with increasing temperature. Typically, the insulation resistance limit at maximum rated temperature is 10% of the 25°C value.

11. Effect of Voltage:

Certain high dielectric constant ceramic capacitors may show variation in values of capacitance and dissipation factor with various levels of applied AC and DC voltages. Such variation is a natural characteristic of ceramic capacitors, and should be considered by the circuit designer.

In general, ceramic capacitors with the lowest dielectric constant (C0G or NP0) are extremely stable, and show little or no variation in capacitance and/or dissipation factor. On the other hand, ceramic capacitors with the highest dielectric constant (Z5U & Y5V) may show significant variation, particularly in capacitance. Other dielectric formulations such as X7R and X5R will show less variation than Y5V, but more than C0G.

The application of AC voltages in the range of 10 to 20 VAC tends to increase the values of both the capacitance and dissipation factor, while higher AC voltages tend to produce decreases in both.

However, the variation of capacitance with applied DC is the parameter of most interest to design engineers. Figure 8 shows typical variation of capacitance with applied DC voltage for some standard dielectrics. As can be seen, the decrease in capacitance is greatest for the Y5V dielectric (the C0G is not plotted, since it would not have a perceptible capacitance nor dissipation factor change.)

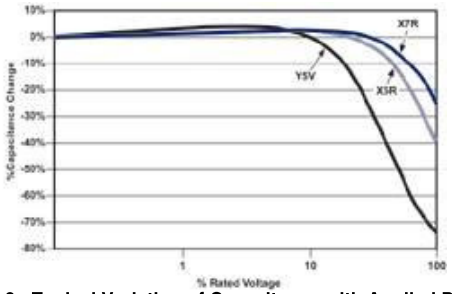


Figure 8 - Typical Variation of Capacitance with Applied DC Voltage

More detailed modelling information on the effect of various voltages on specific capacitor ratings can be obtained by use of the KEMET SPICE models, available for free downloading at our website (www.kemet.com).

12. Effect of Frequency:

Frequency affects both capacitance and dissipation factor. Typical curves for KEMET multilayer ceramic capacitors are shown in Figures 4, 5, 6 and 7.

The variation of impedance with frequency is an important consideration in the application of multilayer ceramic capacitors. Total impedance of the capacitor is

the vector summation of the capacitive reactance, the inductive reactance, and the ESR, as illustrated in Figure 2. As frequency increases, the capacitive reactance decreases. However, the series inductance (L) shown in Figure 1 produces some inductive reactance, which increases with frequency. At some frequency, the impedance ceases to be capacitive and becomes inductive. This point, at the bottom of the V-shaped impedance versus frequency curves, is the self-resonant frequency. At the self-resonant frequency, the reactance is zero, and the impedance consists of the ESR only. At high frequency more detailed models apply - See KEMET SPICE models for such instances.

Typical impedance versus frequency curves for KEMET multilayer ceramic capacitors are shown in Figures 4, 5, 6 and 7.

ENVIRONMENTAL AND PHYSICAL

13. Thermal Shock:
EIA-198, Method 202, Condition B (5 cycles -55° to + 125°C).

14. Life Test:
EIA-198, Method 201, 1000 hours at 200%* of rated voltage at 125°C. (Except 85°C for Z5U, Y5V & X5R).
See Table 4 on page 71 for limits.
*Note: 150% of rated voltage for selected high capacitance X5R values. Please contact factory.

15. Humidity Test:
EIA-198, Method 206, (Except 1000 hours,85°C, 85% RH, Rated Voltage).
See Table 4 on page 71 for limits.

16. Moisture Resistance:
EIA-198, Method 204, Condition B (20 cycles with 50 volts applied.
See Table 4 on page 71 for limits.

17. Solderability:
EIA-198, Method 301 (245°, 5 secs, Sn62 solder) 95% smooth solder on terminations. See page 14 for recommended profiles.

18. Resistance to Soldering Heat:
EIA-198, Method 302, Condition B (260°C, 10 seconds) no leaching of nickel barrier.

19. Terminal Strength:
EIA-198, Method 303, Condition D .

RELIABILITY

20. A well constructed multilayer ceramic capacitor chip is extremely reliable and, for all practical purposes, has no wearout mechanism when used within the maximum voltage and temperature ratings. Most failures occur as a result of mechanical or thermal damage during mounting on the board, or during subsequent testing. Capacitor failure may also be induced by sustained operation at voltages that exceed the rated DC voltage, voltage spikes or transients that exceed the dielectric's voltage capability, sustained operation at temperatures above the maximum rated temperature, internal defects, or excessive temperature rise due to power dissipation. As with any practical device, multilayer ceramic capacitors also possess an inherent, although low, failure rate when operated within rated conditions. The primary failure mode is by short-circuit or low insulation resistance, resulting from cracks or from dielectric breakdown at a defect site. KEMET monitors reliability with a periodic sampling program for selected values. Results are available in our FIT (Failure in Time) report for commercial chips.

21. Storage and Handling:
Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature – reels may soften or warp, and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40 degrees C, and maximum storage humidity not exceed 70% relative humidity. In addition, temperature fluctuations should be minimized to avoid condensation on the parts, and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability, chip stock should be used promptly, preferably within 1.5 years of receipt.

MISAPPLICATION

22. Ceramic capacitors, like any other capacitors, may fail if they are misapplied. Some misapplications include mechanical damage, such as impact or excessive flexing of the circuit board. Others include severe mounting or rework cycles that may also introduce thermal shock. Still others include exposure to excessive voltage, current or temperature. If the dielectric layer of the capacitor is damaged by misapplication, the circuit may fail. The electrical energy of the circuit can be released as heat, which may damage the circuit board and other components as well.

ADDITIONAL INFORMATION

23. Detailed application information can be found in KEMET Engineering Bulletins.

F-2100	Surface Mount-Mounting Pad Dimensions and Considerations
F-2102	Reflow Soldering Process
F-2105	Wave Solder Process
F-2103	Surface Mount Repair
F-2110	Capacitance Monitoring while Flex Testing
F-2111	Ceramic Chip Capacitors “Flex Cracks” - Understanding and Solutions

For analysis of high frequency applications, KEMET has SPICE models of most chip capacitors. Models may be downloaded from KEMET’s website www.kemet.com.

Additional information is also available - See your KEMET representative for details or post your questions to KEMET's homepage on the web http://www.kemet.com.

TABLE 4 – ENVIRONMENTAL LIMITS

Body	Rated DC Voltage	Initial DF (%)	IR (GΩ or ΩF) whichever is less	DF (%) Post Life/ Hum/Moisture Resistance	Cap Shift (% or pf, whichever is greater) Post Life/ Hum/Moisture Resistance	IR (GΩ or ΩF) whichever is less Post Life/ Hum/Moisture Resistance
C0G	200*	0.1	100/1000	0.5	0.3% or ± 0.25 pf	10/100
	100	0.1	100/1000	0.5	0.3% or ± 0.25 pf	10/100
	50	0.1	100/1000	0.5	0.3% or ± 0.25 pf	10/100
	25	0.1	100/1000	0.5	0.3% or ± 0.25 pf	10/100
	16	0.1	100/1000	0.5	0.3% or ± 0.25 pf	10/100
X7R	200*	2.5	100/1000	3.0	± 20%	10/100
	100	2.5	100/1000	3.0	± 20%	10/100
	50	2.5	100/1000	3.0	± 20%	10/100
	25	3.5	100/1000	5.0	± 20%	10/100
	16	3.5	100/1000	5.0	± 20%	10/100
	6.3/10	5.0	100/1000	7.5	± 20%	10/100
X5R	50V all cap values	2.5	100/1000	3.0	± 20%	10/100
	25V all cap values	5.0	100/1000	7.5	± 20%	10/100
	<25<564 cap value	5.0	100/1000	7.5	± 20%	10/100
	>564 cap value	10.0	100/1000	12.0	± 20%	10/100
Z5U	100	4.0	10/100	5.0	± 30%	1/10
	50	4.0	10/100	5.0	± 30%	1/10
	25	4.0	10/100	7.5	± 30%	1/10
Y5V	100	5.0	10/100	7.5	± 30%	1/10
	50	5.0	10/100	7.5	± 30%	1/10
	25	7.0	10/100	10.0	± 30%	1/10
	16	7.0	10/100	10.0	± 30%	1/10
	6.3/10	10.0	10/50	15.0	± 30%	1/5

*200 Volt limits not currently included in EIA-198.

PERFORMANCE CURVES
EFFECT OF FREQUENCY
(See SPICE models for specific ratings.)

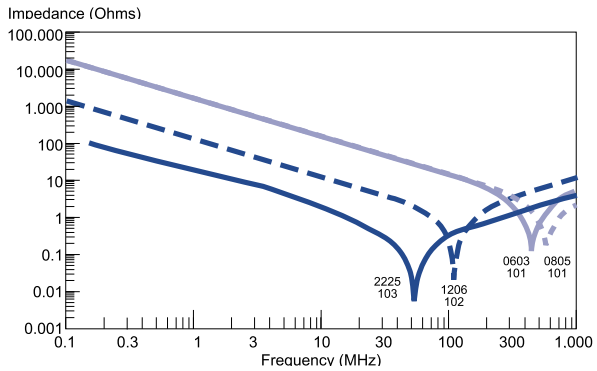


FIGURE 4. Impedance versus Frequency C0G Dielectric

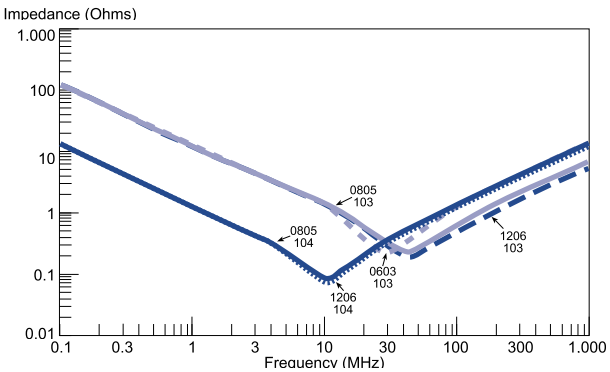


FIGURE 5 Impedance versus Frequency X7R Dielectric

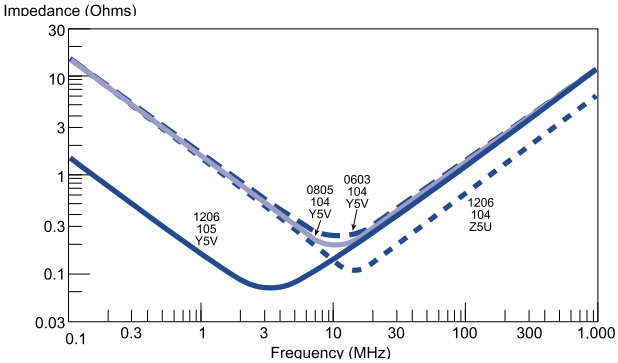


FIGURE 6. Impedance versus Frequency Z5U/Y5V Dielectric

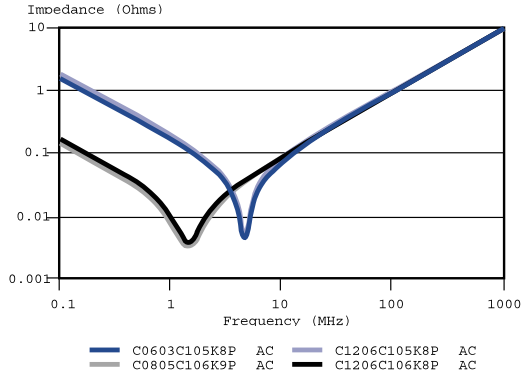


FIGURE 7. Impedence versus Frequency X5R Dielectric